INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	~~10882468~~ 10/822,468	
	Filing Date	2004-04-12	
	First Named Inventor	Mitchell Alsup	
	Art Unit	2183	
	Examiner Name	George D. Zalepa	
	Attorney Docket Number	5500-92000	

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W	6	Hinton, G., et al., "A 0.18-MUM CMOS IA-32 Processor with a 4-GHZ Integer Execution Unit," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, November 2001, pages. 1617-1627.	☐
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W	9	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.	☐
W	10	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.	☐
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W	12	Grant Braught, "Clas #21-Assemblers, Labels & Pseudo Instructions," Dickenson College, Fall Semester 2000, 6 pages.	☐
W	13	U.S. Application Serial No. 10/676,437 filed 10/1/03, Alsup, et al.	☐
W	14	U.S. Application Serial No. 10/615,506 filed 7/8/03, Alsup	☐
W	15	U.S. Application Serial No. 10/755,742 filed 1/12/04, Smaus, et al.	☐

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